

CORPORATE TRAINING WITH 30 DAYS **FREE** TOOL ACCESS

OUR PLATFORM



Intallation is easy and fast with few steps and limited set of package files. simulator package is upgradable from server on a single command.



Simple user interface for design and verification engineers to increase efficiency.



We are committed to provide quick support on our product and timely resolution of reported issues.

WHY CHOOSE US?

- SOFT COPY OF TRAINING MATERIAL
- POST TRAINING 15 DAYS FREE TROUBLE SHOOTING ASSISTANCE THROUGH EMAIL/FTP
- FREE INSTALLATION & ENVIRONMENT SETUP
- AFFORDABLE COSTING

*Special discounts are available for startups and bulk orders.

For further details regarding the training module structure and course fees, please contact us.

CONTACT US

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BASIC SV & TEST BENCH CREATION TRAINING

- Creation of SV based verification environment
- Aggregate datatypes, Classes, Processes, Procedural programming statements
- SV based Test Benches creation

ADVANCED SV TRAINING

- Use of clocking block
- Programs, Packages, Interfaces, Generate construct , Assertions, etc.
- Creation of C++ based VCs using DPI & their integration in VE.

UVM CONCEPTS

- Implementation of coverage model
- Using register layer classes
- Creation of register model
- Integration register model in VE
- Advance Sequence control

ADVANCED UVM & UVC TB

- UVM Phases
- Basic UVM Test Benches architecture
- Transaction Level modeling (TLM)
- Creation of UVC based top level VE.
- VC configuration

